REMARKS

Claims 1-27 are pending in the present application. Claim 28 was previously canceled. Claims 1 and 18 have been amended herein. No new matter has been added. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

Claims 1-4, 7, 9, 14, and 16-17 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Lee (U.S. Patent No. 6,759,335, hereinafter "Lee"). This rejection is hereby respectfully traversed

Lee discloses a buried strap capacitor cell. In the process of forming the buried strap, a collar structure is formed. The collar structure is identified as 55 in Figure 4, for example. A barrier liner 60 is then formed (see, e.g. Figures 6, 7, 8, 10. 11, 12, 13 and14) adjacent the sidewalls of the collar 55. A horizontal layer 62 is formed overlying the top of the liner 60 (see Figure 6) and horizontally forming a buried strap. If the horizontal layer 62 is comprised of HSG as is preferred (see Lee, Col. 3 lines 63-65), then the liner 60 is "optional" because, (as Lee teaches at Col. 3; lines 58-60), HSG will not grow on crystalline silicon. The reference also makes it plain that if another material is used, the liner 60 is formed within the collar divot 55 as a barrier layer to suppress excess out diffusion of dopants and to prevent damage to the silicon layer.

Thus, Applicant concludes that Lee teaches the use of a liner layer in the collar divot 55, or alternatively, if HSG is used as the layer 62, that no HSG will form at the sidewall of the substrate.

The Examiner asserts that Lee anticipates Claim 1, and dependent other claims, of Applicant's claimed methods. The Examiner asserts that Lee discloses fabricating a semiconductor device in a substrate comprising forming a trench having sidewalls in a substrate

10, forming a silicon layer (polysilicon layer 62) along the sidewalls of the trench to continuously cover at least a portion of the sidewalls and performing gas phase doping of the silicon layer (polysilicon layer 62).

Applicant has amended the method of Claim 1 herein to further clarify the meaning of certain steps, and as amended Claim 1 now recites:

> A method of fabricating a semiconductor device in a substrate, the method comprising:
>
> forming a trench having sidewalls and a bottom formed within the substrate, the sidewalls and bottom of the trench being formed of the substrate material;
>
> forming a vertical silicon layer along the sidewalls of the trench to continuously cover at least a portion of the sidewalls, the silicon layer not having a continuous crystalline structure; and
>
> performing gas phase doping so that the silicon layer is doped with a dopant having a concentration of at least $1x10^{19}$ atoms/cm^3.

Applicant respectfully submits that the relied upon reference, Lee, does not show, teach or suggest the required steps of Claim 1.

The Examiner identified substrate 10. The Examiner has not specifically identified what element of the reference he believes is the trench. By identifying layer 62 as the "silicon layer" it appears to Applicant that the collar divot 55, formed by a later recess formation after the deep trench of Lee is formed and filled with material, is the structure the Examiner concludes is the

"trench." The Examiner then asserts that the silicon layer 62 is formed along the sidewalls of the trench.

However, Applicant has carefully reviewed the disclosure of Lee and finds that one of two alternatives is disclosed. In one alternative, as drawn explicitly in Figures 7, 8, 9, 10, 11, 12, 13, and 14, a barrier layer of silicon nitride is formed in the divot 55. The silicon layer 62 is then formed and is formed horizontally over the silicon electrode 54 and is not formed along the sidewalls of the trench. In another alternative, HSG is used for layer 62 and Lee discloses that the HSG will not form a layer continuously over the sidewalls, as HSG is not capable of forming on crystalline silicon (Col. 3 lines 58-60) thus the liner is not required for that embodiment.

Applicant concludes that Lee never discloses forming a vertical silicon layer along the sidewalls of the trench to continuously cover at least a portion of the sidewalls, the silicon layer not having a continuous crystalline structure..., in contrast to the Examiner's remarks of the Office Action. The reference instead discloses filling the collar divot 55 with a barrier liner, and then depositing the silicon layer horizontally. Applicant believes that the required method steps are not disclosed or suggested, and that Claim 1 is therefore allowable over the reference. Reconsideration and allowance are requested.

Claims 2-4, 7, 9, 14, and 16-17 were similarly rejected. These dependent method claims add additional steps to the method of Claim 1. As the parent claim is now believed to be allowable, these dependent method claims are also believed to recite allowable steps and to be allowable over the rejection. Reconsideration and allowance are therefore requested.

Claims 5-6, 8, 10-13, and 18-24 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee, in view of Chung et al. (U.S. Patent No. 6,734,106, hereinafter "Chung"). This rejection is also hereby respectfully traversed.

Claims 5-6, 8 and 10-13 depend from and add additional steps to the method of Claim 1. As argued above, Claim 1 is now believed to be allowable over the Lee reference.

Chung is added to Lee by the Examiner because the Lee reference admittedly does not disclose certain process conditions required by the claims. Chung is said to disclose these process conditions.

Without addressing whether or not the required motivations to combine Lee and Chung in the manner suggested by the Examiner are present, Applicant responds that the combination does not obviate claims depending from Claim 1. As argued above, Claim 1 recites methods not disclosed by the primary reference Lee. The dependent claims add additional method steps to the allowable method of Claim 1. Chung may provide particular process conditions but nevertheless the relied upon references, taken singly or in combination, fail to disclose the method of the independent claim and thus, each dependent claim also recites steps that are not shown, taught or suggested by the references. Accordingly, Applicant believes that these dependent claims are allowable. Reconsideration and allowance are therefore requested.

Claims 18-24 are similarly rejected over the Lee in view of Chung in combination. Claim 18 is amended herein to clarify the steps and now recites:

> A method of fabricating a semiconductor device in a substrate, the method comprising:
>
> forming a trench having sidewalls and a bottom within the substrate, the sidewalls and the bottom of the trench being formed of the substrate material;
>
> lining the sidewalls with a node dielectric and forming sidewalls of the node dielectric;

depositing a vertical silicon layer to continuously cover at least a portion of the sidewalls of the node dielectric, the vertical silicon layer not having a continuous crystalline structure; and

performing gas phase doping in a reaction chamber by:

flowing a dopant precursor gas in the reaction chamber at a rate of between 100-300 sccm,

heating the reaction chamber to a temperature of between 850-1000°C, and

pressurizing the reaction chamber to a pressure of between 1-100 Torr, wherein the gas phase doping results in the silicon layer being doped with a dopant having a concentration of at least $1x10^{19}$ atoms/cm^3.

As argued above with respect to Claim 1, the Lee reference does not show, suggest or describe the method of Claim 18 in particular the reference does not disclose forming a silicon layer over a node dielectric sidewall and then gas phase doping the silicon layer as required.

The Examiner remarks that the silicon layer of Lee, layer 62, is formed to cover at least a portion of the node dielectric, however, first the Applicant submits that Lee actually teaches a liner or barrier layer of silicon nitride 60 between the layer of silicon 62 and the dielectric 20, see the arguments above with respect to Claim 1, and see also Lee at Figures 6, 7, 8, 9, 10, 11, 12, 13, for example. Secondly, Applicant further submits that the Lee reference does not teach forming the silicon layer over the sidewalls of the node dielectric, as recited in Claim 18.

The secondary reference to Chung is recited by the Examiner for certain process conditions also admittedly not described in Lee. Again without discussing whether the required motivation to combine these references is present, Applicant submits that neither reference nor the combination proposed by the Examiner shows, teaches, or suggests the steps of independent claim 18. Accordingly, reconsideration and allowance are requested for Claim 18.

Claims 19-24 depend from and recite additional method steps on the method of Claim 18. As the parent claim is now believed to be allowable over the rejection, these dependent claims also necessarily recite allowable methods and are also believed to be allowable. Accordingly reconsideration and allowance are requested.

Claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Cheong (U.S. Publication No. 2003/0186533, hereinafter "Cheong"). This rejection is also hereby respectfully traversed.

Claim 15 depends from Claim 1 and adds the step of ex-situ processing. The Examiner admits that Lee does not provide these steps and recites Cheong for the particular step recited by Claim 15.

Applicant submits however that as argued above, Claim 1, the parent claim, is allowable over Lee. The combination of Lee with Cheong does not cure the deficiencies in Lee with respect to Claim 1, and Claim 15 depends from and incorporates the allowable steps of Claim 1. Accordingly neither Lee nor Cheong, or the combination of both proposed by the Examiner, anticipates or obviates the method of Claim 15.

Applicant concludes that Claim 15 is allowable over the rejection. Reconsideration and allowance are therefore respectfully requested.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge, or credit any overpayment, Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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